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DATE: Thursday, February 17, 2005

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☐ 1. Document ID: US 6641675 B2

Using default format because multiple data bases are involved.

L8: Entry 1 of 3 File: USPT Nov 4, 2003

US-PAT-NO: 6641675
DOCUMENT-IDENTIFIER: US 6641675 B2

TITLE: Method and apparatus for immersion treatment of semiconductor and other devices

DATE-ISSUED: November 4, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dryer; Paul William	Gilbert	AZ		
Tirendi; Richard Scott	Phoenix	AZ		
Sundin; James Bradley	Chandler	AZ		

US-CL-CURRENT: 134/1; 134/1.3, 134/10, 134/25.4, 134/28, 134/3, 134/30, 134/902

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 2. Document ID: US 6284055 B1

L8: Entry 2 of 3 File: USPT Sep 4, 2001

US-PAT-NO: 6284055
DOCUMENT-IDENTIFIER: US 6284055 B1

TITLE: Method and apparatus for immersion treatment of semiconductor and other devices

DATE-ISSUED: September 4, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dryer; Paul William	Gilbert	AZ		
Tirendi; Richard Scott	Phoenix	AZ		
Sundin; James Bradley	Chandler	AZ		

US-CL-CURRENT: 134/10; 134/111, 134/25.4, 134/902

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ABSTRACT:

Method and apparatus for cleaning semiconductor devices and other workpieces using an aqueous rinse solution which is de-oxygenated by passing the aqueous rinse solution and a carrier gas through an osmotic membrane degasifier. A cleaning chamber is also disclosed for carrying out the cleaning method.

20 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 3. Document ID: US 6244280 B1

L8: Entry 3 of 3 File: USPT Jun 12, 2001

US-PAT-NO: 6244280
DOCUMENT-IDENTIFIER: US 6244280 B1

TITLE: Method and apparatus for immersion treatment of semiconductor and other devices

DATE-ISSUED: June 12, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dryer; Paul William	Gilbert	AZ		
Tirendi; Richard Scott	Phoenix	AZ		
Sundin; James Bradley	Chandler	AZ		

US-CL-CURRENT: 134/100.1; 134/102.1, 134/111, 134/902, 210/321.79

ABSTRACT:

Method and apparatus for cleaning semiconductor devices and other workpieces using an aqueous rinse solution which is de-oxygenated by passing the aqueous rinse solution and a carrier gas through an osmotic membrane degasifier. A cleaning chamber is also disclosed for carrying out the cleaning method.

6 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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Term	Documents

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DRIPPING	32029
DRIPPINGS	2144
(5 AND DRIPPING).PGPB,USPT,EPAB,JPAB,DWPI,TDBD.	3
(L5 AND DRIPPING).PGPB,USPT,EPAB,JPAB,DWPI,TDBD.	3

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L3: Entry 1 of 29 File: PGPB Nov 4, 2004

PGPUB-DOCUMENT-NUMBER: 20040216762
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040216762 A1

TITLE: Method for polymer residue removal following metal etching

PUBLICATION-DATE: November 4, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Lo, Chi-Hsin	Hsin-Chu		TW	
Chen, Fei-Yun	Hsin-Chu		TW	

US-CL-CURRENT: 134/2; 134/29, 134/36

CLAIMS:

What is claimed is:

1. A method for removing polymer containing residues from a semiconductor wafer including metal containing features comprising the steps of: providing a semiconductor wafer having a process surface including metal containing features said process surface at least partially covered with polymer containing residues; and subjecting the semiconductor wafer to a series of cleaning steps including sequentially exposing the process surface to at least one primary solvent and at least one intermediate solvent the at least one intermediate solvent comprising an ammonium nitrate containing solution.

2. The method of claim 1, wherein the step of providing a semiconductor wafer includes following a plasma metal etching process for etching the metal containing features.

3. The method of claim 1, wherein the primary solvent is a wet etchant solution.

4. The method of claim 3, wherein the wet etchant solution includes at least one of Dimethyl-sulphur-oxide, Mono-Ethyl-Amine and catechol.

5. The method of claim 1, wherein the ammonium nitrate containing solution includes a concentration of about 0.5 percent to about 2 percent by volume of ammonium nitrate.

6. The method of claim 5, wherein the ammonium nitrate containing solution includes a concentration of about 1 percent by volume of ammonium nitrate.

7. The method of claim 5, wherein the ammonium nitrate containing solution includes deionized water and ammonium nitrate.

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8. The method of claim 1, wherein exposing the process surface includes at least one of immersing and spraying the process surface.

9. The method of claim 8, wherein immersing the process surface includes immersing the semiconductor wafer in at least one solution bath of the at least one intermediate solvent for a period of about 5 minutes to about 15 minutes.

10. The method of claim 9, wherein the at least one solution bath is simultaneously agitated while immersing the semiconductor wafer.

11. The method of claim 1, wherein the series of cleaning steps includes exposing the process surface to at least one rinsing solution following the step of exposing the process surface to at least one intermediate solvent.

12. The method of claim 1, wherein the ammonium nitrate containing solution is maintained at a temperature of from about 75 degrees Centigrade to about 150 degrees Centigrade.

13. A method for removing polymer containing residues from a semiconductor wafer including following a reactive ion metal etching process comprising the steps of: providing a semiconductor wafer having a process surface including metal containing features said process surface at least partially covered with polymer containing residues; and subjecting the semiconductor wafer to a series of cleaning steps including sequentially exposing the process surface to at least one primary solvent for wet etching and at least one intermediate solvent the at least one intermediate solvent comprising an ammonium nitrate solution having a concentration of ammonium nitrate between about 0.5 percent and about 2 percent by volume.

14. The method of claim 14, wherein the primary solvent includes at least one of Dimethyl-sulphur-oxide, Mono-Ethyl-Amine and catechol.

15. The method of claim 13, wherein the ammonium nitrate solution includes a concentration of about 1 percent by volume of ammonium nitrate.

16. The method of claim 15, wherein the ammonium nitrate solution includes deionized water and ammonium nitrate.

17. The method of claim 13, wherein the step including exposing the process surface includes at least one of immersing and spraying the process surface.

18. The method of claim 17, wherein the step including exposing the process surface includes immersing the semiconductor wafer in at least one solution bath of the least one intermediate solvent for a period of about 5 minutes to about 15 minutes.

19. The method of claim 18, wherein the at least one solution bath is maintained at a temperature of from about 75 degrees Centigrade to about 150 degrees Centigrade.

20. The method of claim 13, wherein the series of cleaning steps includes exposing the process surface to at least one rinsing solution following the step of exposing the process surface to at least one intermediate solvent.

21. The method of claim 13, wherein the series of cleaning steps is performed in a wet chemical bench process line having a controlled ambient environment.

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☐ 1. Document ID: US 6837978 B1

L5: Entry 1 of 18 File: USPT Jan 4, 2005

US-PAT-NO: 6837978
DOCUMENT-IDENTIFIER: US 6837978 B1

TITLE: Deposition uniformity control for electroplating apparatus, and associated method

DATE-ISSUED: January 4, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hey; H. Peter W.	Sunnyvale	CA		
Dordi; Yezdi N.	Palo Alto	CA		
Olgado; Donald J. K.	Palo Alto	CA		
Denome; Mark	San Jose	CA		

US-CL-CURRENT: 205/84; 204/224R, 204/227, 204/229.8, 204/275.1, 205/96

ABSTRACT:

A method and associated apparatus for electro-chemically depositing a metal film on a substrate having a metal seed layer. The apparatus comprises a substrate holder that holds the substrate. The electrolyte cell receives the substrate in a processing position. The actuator is connected to the substrate holder and adjustably positions the substrate relative to the electrolyte cell. The method involves electro-chemically depositing a metal film on a substrate having a metal seed layer comprising disposing the substrate in an electrolyte cell that is configured to receive the substrate. The method comprises adjustably positioning the substrate relative to the electrolyte cell.

30 Claims, 31 Drawing figures
Exemplary Claim Number: 16
Number of Drawing Sheets: 25

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 2. Document ID: US 6824622 B2

L5: Entry 2 of 18 File: USPT Nov 30, 2004

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US-PAT-NO: 6824622
DOCUMENT-IDENTIFIER: US 6824622 B2

TITLE: Cleaner and method for removing fluid from an object

DATE-ISSUED: November 30, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Liu; Yi-Chang	Kaohsiung			TW
Chang; Chia-Chen	Kaohsiung			TW
Dai; Yuan-Mou	Taoyuan			TW

US-CL-CURRENT: 134/30; 134/18, 134/25.4, 134/32, 134/37, 134/56R, 134/57R, 134/58R, 134/902, 134/95.2, 134/95.3

ABSTRACT:

A cleaner and method for removing excess residual cleaning fluid from an object, particularly a semiconductor wafer, before or as the wafer is removed from a cleaning chamber of a CMP cleaner, for example. Typically, a purge bar is mounted on each side of the cleaning chamber for blowing nitrogen or clean, dry air (CDA) against a corresponding surface of the wafer to remove the excess cleaning fluid from the wafer. The purge bars may be connected to a controller for a wafer transfer device which removes the wafer from the cleaning chamber, such that the purge bars are actuated as the wafer transfer device begins to remove the wafer from the chamber.

20 Claims, 5 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

3. Document ID: US 6800169 B2

L5: Entry 3 of 18 File: USPT Oct 5, 2004

US-PAT-NO: 6800169
DOCUMENT-IDENTIFIER: US 6800169 B2

TITLE: Method for joining conductive structures and an electrical conductive article

DATE-ISSUED: October 5, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Liu; Kuo-Chuan	Fremont	CA		
Lee; Michael G.	San Jose	CA		

US-CL-CURRENT: 156/292; 156/295, 156/309.6, 228/180.22, 228/193, 228/195,

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257/E21.505, 29/830, 438/618

ABSTRACT:

Embodiments of the invention include a method comprising disposing a thin metallic layer having a low melting temperature between one end of a conductive post on a substrate and a conducting structure on an opposing substrate. Heated platens in contact with the substrates can apply pressure and heat to the thin metallic layer and cause it to be entirely consumed and subsequently transformed into a bonding layer having a melting temperature higher than the melting temperature of the original thin metallic layer. Prior to, during, or after the conductive post is bonded to the conducting structure, the region around the conductive post and between the substrates may be filled with a dielectric material, such as polyimide.

18 Claims, 168 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 48

4. Document ID: US 6662673 B1

L5: Entry 4 of 18 File: USPT Dec 16, 2003

US-PAT-NO: 6662673
DOCUMENT-IDENTIFIER: US 6662673 B1

TITLE: Linear motion apparatus and associated method

DATE-ISSUED: December 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Olgado; Donald J. K.	Palo Alto	CA		

US-CL-CURRENT: 74/490.01; 204/279, 29/428

ABSTRACT:

A guide apparatus comprising a plurality of guide linkages. Each one of the plurality of guide linkages comprises a pair of linkage members, each pair of the linkage members are rotatably connected about a guide pivot axis. The guide pivot axis of each guide linkage is arranged in a direction opposed to the direction of the guide pivot axis of the remainder of the guide linkages. In one aspect, each guide linkage is arranged between a robot platform or a cassette and a base such that extending each of the plurality of guide linkages acts to linearly displace the robot platform relative to the base while limiting tilting of the robot platform or the cassette. In another aspect a robot can extend its end effectors while limiting tilting of the end effectors.

31 Claims, 38 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 28

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 5. Document ID: US 6613692 B1

L5: Entry 5 of 18 File: USPT Sep 2, 2003

US-PAT-NO: 6613692
DOCUMENT-IDENTIFIER: US 6613692 B1

TITLE: Substrate processing method and apparatus

DATE-ISSUED: September 2, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Toshima; Takayuki	Futaba-Cho			JP
Ueno; Kinya	Nirasaki			JP
Yamasaka; Miyako	Nagasaka-Cho			JP
Tsutsumi; Hideyuki	Kawasaki			JP
Iino; Tadashi	Nirasaki			JP
Kamikawa; Yuji	Koshi-Machi			JP

US-CL-CURRENT: 438/745; 257/E21.255, 438/706, 438/711, 438/714, 438/715, 438/719, 438/725

ABSTRACT:

Semiconductor wafers are cleaned by placing the semiconductor wafers in a processing vessel, forming a pure water film on the surfaces of the wafers, forming an ozonic water film by dissolving ozone gas in the pure water film, and removing resist films formed on the wafers by the agency of the ozonic water film. The pure water film is formed by condensing steam on the surfaces of the wafers. The resist films formed on the surfaces of the wafers can be removed by also using hydroxyl radicals produced by interaction between steam and ozone gas supplied into the processing vessel. Thus, the resist films can be removed highly effectively.

13 Claims, 41 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 30

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 6. Document ID: US 6582578 B1

L5: Entry 6 of 18 File: USPT Jun 24, 2003

US-PAT-NO: 6582578
DOCUMENT-IDENTIFIER: US 6582578 B1
**** See image for Certificate of Correction ****

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TITLE: Method and associated apparatus for tilting a substrate upon entry for metal deposition

DATE-ISSUED: June 24, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dordi; Yezdi N.	Palo Alto	CA		
Stevens; Joseph J.	San Jose	CA		
Sugarman; Michael N.	San Francisco	CA		

US-CL-CURRENT: 205/80; 204/212, 204/224R, 204/225, 205/134, 205/669, 427/430.1

ABSTRACT:

An electro-chemical plating system is described. A method is performed by the electro-chemical plating system in which a seed layer formed on a substrate is immersed into an electrolyte solution. In one aspect, a substrate is immersed in the electrochemical plating system by tilting the substrate as it enters the electrolyte solution to limit the trapping or formation of air bubbles in the electrolyte solution between the substrate and the substrate holder. In another aspect, an apparatus is provided for electroplating that comprises a cell, a substrate holder, and an actuator. The actuator can displace the substrate holder assembly in the x and z directions and also tilt the substrate. In another aspect, a method is provided of driving a meniscus formed by electrolyte solution across a surface of a substrate. The method comprises enhancing the interaction between the electrolyte solution meniscus and the surface as the substrate is immersed into the electrolyte solution.

28 Claims, 45 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 31

7. Document ID: US 6578592 B1

L5: Entry 7 of 18 File: USPT Jun 17, 2003

US-PAT-NO: 6578592
DOCUMENT-IDENTIFIER: US 6578592 B1

TITLE: Processing apparatus with horizontally movable enclosing element

DATE-ISSUED: June 17, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kamikawa; Yuji	Tosu			JP
Orii; Takehiko	Nirasaki			JP
Kohama; Kyouji	Tosu			JP

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US-CL-CURRENT: 134/200; 118/501, 134/902

ABSTRACT:

A cleaning system has a movable outer tubular member (26) and a movable inner tubular member (27). A bottom part of the inner tubular (27) is inclined. A first drain pipe (47) is connected to the inner tubular member (27). The first drain pipe (47) has an end part slidably inserted into a second drain pipe (76).

23 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 14

☐ 8. Document ID: US 6517418 B2

L5: Entry 8 of 18 File: USPT Feb 11, 2003

US-PAT-NO: 6517418
DOCUMENT-IDENTIFIER: US 6517418 B2

TITLE: Method of transporting a semiconductor wafer in a wafer polishing system

DATE-ISSUED: February 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Engdahl; Erik H.	Livermore	CA		
Ferri, Jr.; Edward T.	Gilroy	CA		
Krusell; Wilbur C.	Palo Alto	CA		
Jairath; Rahul	San Jose	CA		

US-CL-CURRENT: 451/41; 257/E21.23, 257/E21.244, 451/332, 451/63

ABSTRACT:

A system and method for planarizing a plurality of semiconductor wafers is provided. The method includes the steps of processing each wafer along the same process path using at least two polishing stations to each partially planarize the wafers. The system includes an improved process path exchanging a detachable wafer carrying head with spindles at each processing point and conveying the detached wafer carrying heads in a rotary index table between processing points. The system also provides for improved polishing accuracy using linear polishers having pneumatically adjustable belt tensioning and aligning capabilities.

15 Claims, 31 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 23

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9. Document ID: US 6416385 B2

L5: Entry 9 of 18 File: USPT Jul 9, 2002

US-PAT-NO: 6416385
DOCUMENT-IDENTIFIER: US 6416385 B2
** See image for Certificate of Correction **

TITLE: Method and apparatus for polishing semiconductor wafers

DATE-ISSUED: July 9, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ferri, Jr.; Edward T.	Gilroy	CA		
Green; Randall L.	Watsonville	CA		
Pant; Anil K.	Santa Clara	CA		

US-CL-CURRENT: 451/10; 257/E21.23, 257/E21.244, 451/11, 451/297, 451/307, 451/311, 451/36, 451/41

ABSTRACT:

A system and method for planarizing a plurality of semiconductor wafers is provided. The method includes the steps of processing each wafer along the same process path using at least two polishing stations to each partially planarize the wafers. The system includes an improved process path exchanging a detachable wafer carrying head with spindles at each processing point and conveying the detached wafer carrying heads in a rotary index table between processing points. The system also provides for improved polishing accuracy using linear polishers having pneumatically adjustable belt tensioning and aligning capabilities.

19 Claims, 31 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 23

10. Document ID: US 6336845 B1

L5: Entry 10 of 18 File: USPT Jan 8, 2002

US-PAT-NO: 6336845
DOCUMENT-IDENTIFIER: US 6336845 B1

TITLE: Method and apparatus for polishing semiconductor wafers

DATE-ISSUED: January 8, 2002

INVENTOR-INFORMATION:

h e b b g e e e f e ef b e

NAME	CITY	STATE	ZIP CODE	COUNTRY
Engdahl; Erik H.	Livermore	CA		
Ferri, Jr.; Edward T.	Gilroy	CA		
Krusell; Wilbur C.	Palo Alto	CA		
Jairath; Rahul	San Jose	CA		
Green; Randall L.	Watsonville	CA		
Pant; Anil	Santa Clara	CA		

US-CL-CURRENT: 451/41; 257/E21.23, 257/E21.244, 451/285, 451/287, 451/307, 451/332, 451/59

ABSTRACT:

A system and method for planarizing a plurality of semiconductor wafers is provided. The method includes the steps of processing each wafer along the same process path using at least two polishing stations to each partially planarize the wafers. The system includes an improved process path exchanging a detachable wafer carrying head with spindles at each processing point and conveying the detached wafer carrying heads in a rotary index table between processing points. The system also provides for improved polishing accuracy using linear polishers having pneumatically adjustable belt tensioning and aligning capabilities.

25 Claims, 31 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 23

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